SY7072

1.8V Minimum Input and 5. 5V Maximum Output High Efficiency 2A Valley Current Synchronous Boost

Advanced Design Specification

General Description

SY7072 is a high efficient, synchronous, step-up Boost converter designed for one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline Ni-Cd or Ni-MH battery powered applications. It can convert down to 1.8V input voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch.

SY7072 can disconnect the output from input during the shutdown mode. When input voltage exceeds the regulated output voltage, SY7072 enters bypass mode automatically.

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 1.8V to 5.5V
- Auto Output Capacitor Discharge When Shutdown
- Min 2A Valley Current Limit
- 5μA Typical Quiescent Current
- Load Disconnect During Shutdown
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 3.3V Output: 100/170mΩ
- Output OVP
- Auto Bypass Mode When $V_{IN} \geq V_{OUT}$
- Compact Package SOT23-6

Ordering Information

SY7072 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7072ABC	SOT23-6	----

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment.

Typical Applications

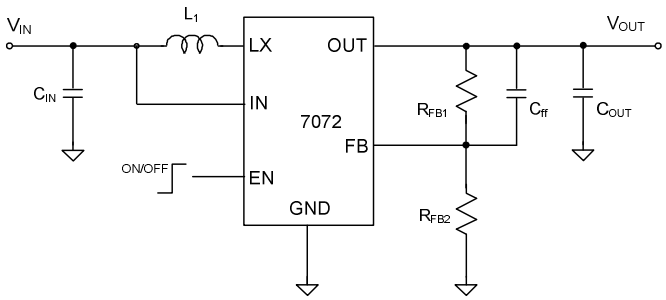


Figure 1. Schematic Diagram

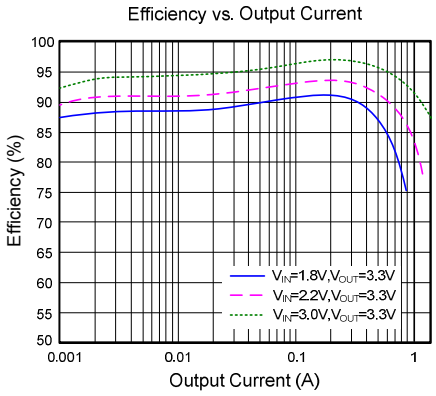
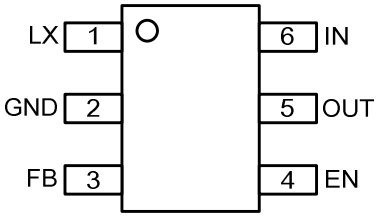


Figure 2. Efficiency vs. Load Current

Pinout (top view)



(SOT23-6)

Top mark: **Uy*xyz* *for SY7072ABC*** (Device code: Uy, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
LX	1	Inductor node. Connect an inductor between the IN pin and the LX pin.
GND	2	Ground pin.
FB	3	Feedback pin. Connect a resistor R_{FB1} between OUT and FB, and a resistor R_{FB2} between FB and GND to program the output voltage. V_{OUT}=1.2V× (R_{FB1}/R_{FB2}+1).
EN	4	Enable pin. Pull high to turn on. Do not leave it floating.
OUT	5	Output pin. Decouple this pin to the GND pin with a minimum of 22µF ceramic capacitor.
IN	6	Input pin.

Block Diagram

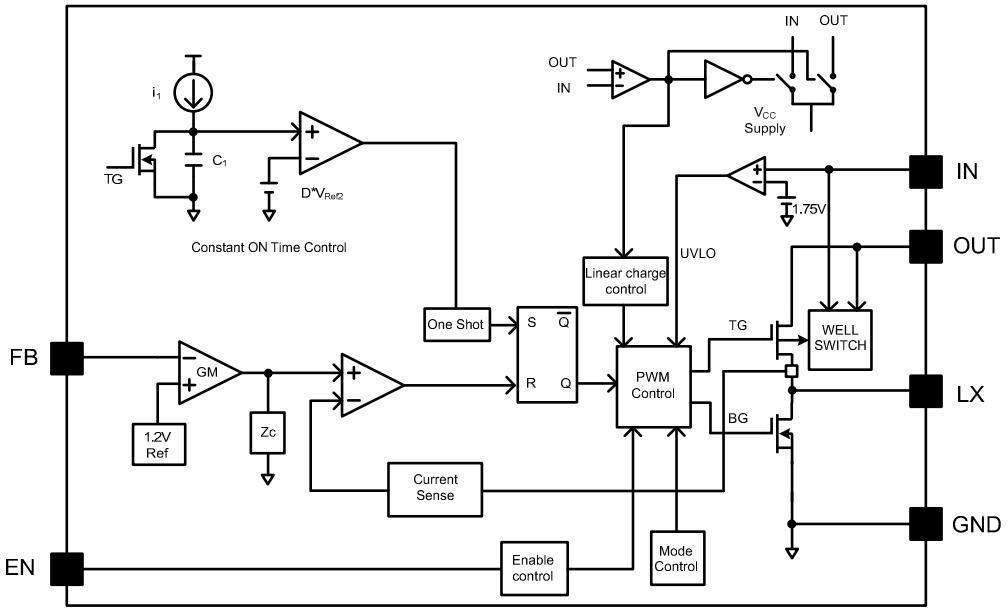


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

All Pins ---------- 6.0V
Power Dissipation, P_D@ T_A=25°C SOT23-6---------- 1W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 100°C/W
θ_{JC} ---------- 30°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 1.8V to 5.5V
OUT---------- 1.8V to 5.5V
EN ---------- 0V to V_{OUT}+0.3V
All other pins ---------- 0-5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =2.4V, V_{OUT}=3.3V, I_{OUT}=500mA, T_A = 25°C, unless otherwise specified)

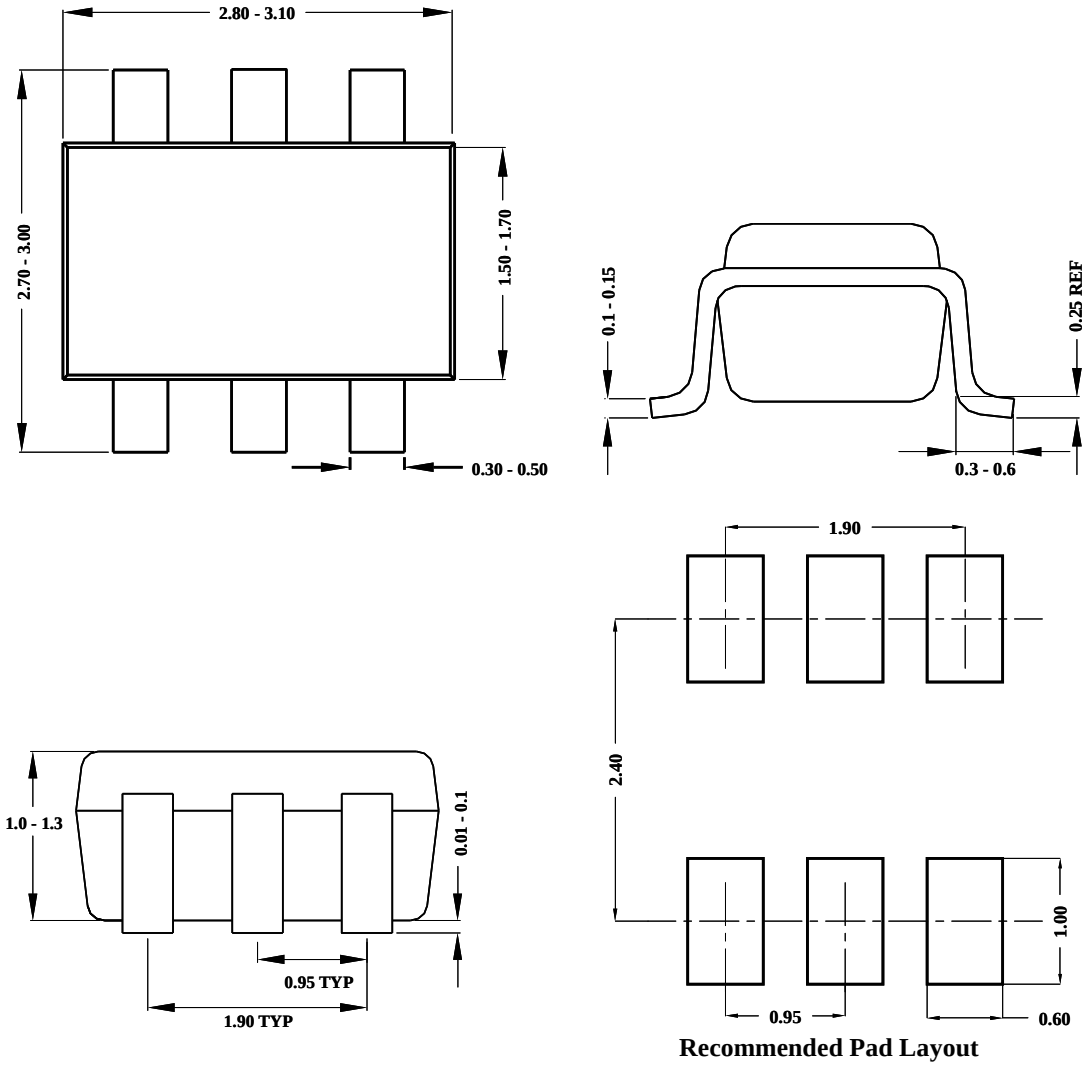
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		V_{IN}		1.8		5.5	V
Input UVLO Threshold		V_{UVLO}			1.65	1.75	V
Input UVLO Hysteresis		V_{HYS}			0.1		V
Quiescent Current	V_{IN}	I_Q	V_{FB}=1.3V,V_{EN}=V_{IN}=2V, V_{OUT}=3.4V		1		μA
	V_{OUT}				5		μA
Shutdown Current		I_{SHDN}	V_{EN}=0V,V_{IN}=2.4V		0.1	1	μA
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	mV
Output Discharge Current		I_{DIS}	Vo=3.3V		44		mA
Output Discharge Resistance		R_{DIS}			75		Ω
Low Side Main FET R_{ON}		$R_{DS(ON)1}$			170		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$			100		mΩ
EN Input Voltage High		$V_{EN,H}$		1.2			V
EN Input Voltage Low		$V_{EN,L}$				0.4	V
EN Leakage Current		$I_{EN,LK}$	V_{EN}=3.3V	-1		1	μA
Min ON Time		$t_{ON,MIN}$			60		ns
Min OFF Time		$t_{OFF,MIN}$			140		ns
Soft-Start Time		t_{SS}			1		ms
Switching Frequency		F_{SW}	V_{OUT}=3.3V, CCM		1		MHz
Valley Current Limit		$I_{LMT,VAL}$		2			A
Output Over Voltage Threshold		V_{OVP}			5.8		V
Output Over Voltage Hysteresis		$V_{OVP,HYS}$			0.3		V
Thermal Shutdown Temperature		T_{SD}			150		˚C
Thermal Shutdown Hysteresis		T_{HYS}			20		˚C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

SOT23-6 Package Outline & PCB Layout Design

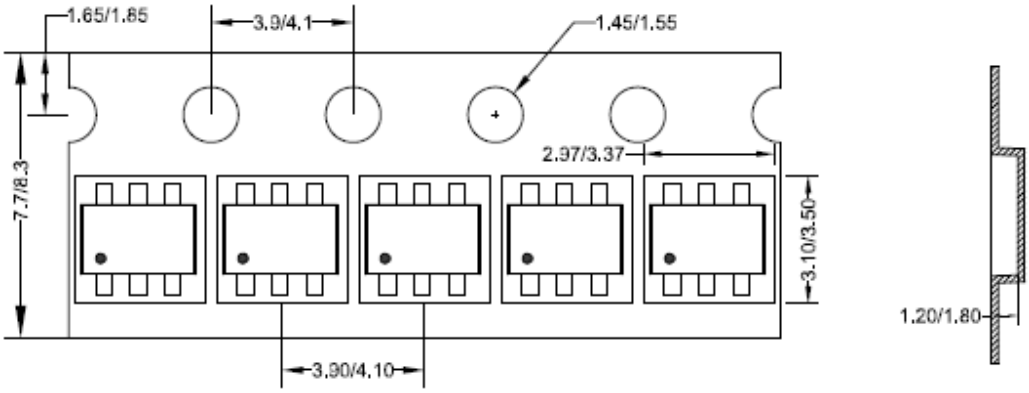


Recommended Pad Layout

Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

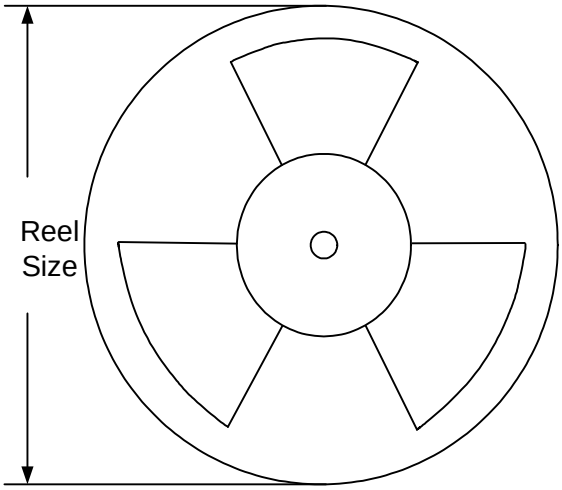
Taping & Reel Specification

1. Taping orientation for packages（SOT23-6）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA